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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., AND AEROFLEX COLORADO SPRINGS, INC.

Defendants.

SYNOPSYS, INC.,

Plaintiff,

vs.

RICOH COMPANY, LTD.,

Defendant.

Case No. C03-04669 MJJ (EMC)

Case No. C03-02289 MJJ (EMC)

[PROPOSED] ORDER RE SUBPOENAS AND INFORMAL DOCUMENT REQUESTS PURSUANT TO ORDER OF AUGUST 24, 2006 AND EXPLANATION THEREOF

Judge: Hon. Edward M. Chen

[PROPOSED] ORDER

Pursuant to this Court's August 24, 2006 Order (*Synopsys* Dkt. No. 440), the parties have met and conferred to narrow the scope of the subpoenas and informal requests that were the subject of Ricoh's Motion For Protective Order (*Synopsys* Dkt. No. 409). The parties were unable to resolve their differences and each side has submitted its proposed limitations to the informal document requests and Rule 45 subpoenas. The Court, having considered the submissions of the parties, and good cause appearing therefor, hereby adopts the limitations set forth by the Defendants.

IT IS HEREBY ORDERED that:

1) The informal document requests are limited by restricting each category to documents that relate to or discuss in any way logic synthesis (including any discussion of the inputs to logic synthesis tools), register transfer level ('RTL'), or computer or circuit architecture.

2) Defendants shall not seek enforcement of Michigan Request No. 4, MIT Request No. 3, and Yale Request No. 3.

3) Defendants shall inform the subpoenaed parties that the remaining requests are limited to documents that relate to or discuss in any way logic synthesis (including any discussion of the inputs to logic synthesis tools), register transfer level ('RTL'), or computer or circuit architecture.

4) Defendants shall not enforce any third party subpoena beyond the scope set forth in point 3 above.

IT IS SO ORDERED.

Dated: _____ _____

EXPLANATION

In their opposition to Ricoh's motion, Defendants responded to Ricoh's overbreadth objection as the clear afterthought it was, included in a litany of (since rejected) reasons raised to prevent Defendants from having access to what is likely to prove to be highly relevant and quite damaging information to Ricoh. Defendants should have made the reasonableness of its requests more clear to

the Court in its opposition, and they provide some brief additional comments here because it is important to fully understand the issues to resolve this dispute.

Defendants' proposal to strike certain requests and limit the remaining requests to documents "that relate to or discuss in any way logic synthesis (including any discussion of the inputs to logic synthesis tools), register transfer level ('RTL'), or computer or circuit architecture" is completely "focus[ed] on the matters fairly raised by the deposition testimony of this expert." (Order at 4:9-10.) Ricoh, in contrast, asserts the limitation should be "define[] or otherwise refer[] to register transfer level ('RTL')." Ricoh's language is too narrow, particularly because the third parties have no context regarding this dispute and would not easily comprehend the scope of this limitation.

In the context of this case, whether or not something is "RTL" or "not RTL" relates to whether or not the inputs to a logic synthesis tool (such as the accused Verilog and VHDL Customer Defendant inputs to Synopsys' Design Compiler) meet the definition of "architecture independent actions and conditions" — the claim limitation construed by Judge Jenkins to mean "functional or behavioral aspects of a portion of a circuit (or circuit segment) that does not imply a set architecture, structure, or implementing technology, but excludes the use of register-transfer level descriptions as taught in Darringer." (Claim Construction Order at 12:16-19.) Indeed, Dr. Papaefthymiou was hired by Ricoh for the sole purpose of opining on this single issue. Thus, any discussion of RTL in this case relates to whether or not inputs to a computer aided design system or logic synthesis tool meet or do not meet the definition of "architecture independent actions and conditions"; this is the scope of information that is relevant for purposes of impeachment of Dr. Papaefthymiou.

With regard to the alleged burden on third parties and/or overbreadth, it is significant to note that the evidence shows that Dr. Papaefthymiou has only taught 7 courses and submitted approximately 10 invention disclosures. *See, e.g.*, Andelman Decl., Ex. C (Papaefthymiou CV) at 1, 3, 13. With the potential exception of a course entitled "Advanced Algorithms" (MIT Req. 2), all of the courses are directly relevant to the subject matter of Dr. Papaefthymiou's report[1] — whether the

[1] For example, Dr. Papaefthymiou's Computer Systems course at Yale included implementing a system in Verilog. Moreover, the very titles of two of Dr. Papaefthymiou's courses at the University of Michigan — Computer-Aided Design

(Continued...)

Defendants' Verilog and VHDL inputs to Design Compiler, a logic synthesis tool, are architecture independent. In fact, Dr. Papaefthymiou's students use Synopsys' Design Compiler to design ASICs and his research and teaching efforts are focused on relevant issues as set forth in his expert report (and confirmed in his deposition):

> My research interests are in the areas of computer-aided design, and VLSI (including custom and ASIC design). I have taught senior and graduate-level courses in logic synthesis and VLSI design. My research and teaching activities routinely involve hardware description languages, commercial design tools by Synopsys and other vendors, ASIC designs, and ASIC design processes at all levels of abstraction.

Expert Report at 1.

In view of these facts, Defendants respectfully suggest that their proposed limitation is sufficient to limit the discovery to material fairly raised by Dr. Papaefthymiou's deposition.

Dated: August 29, 2006

Respectfully submitted,

HOWREY, LLP

By: /s/ Ethan B. Andelman
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(...Continued)

of Embedded Systems and Logic Circuit Synthesis — show that these courses are directly relevant to the subject matter of the patent, areas in dispute in this litigation, and the specific area of dispute on which Dr. Papaefthymiou is opining.